Overview
Wafer-level Packaging (WLCSP) is the technology of packaging and testing an integrated circuit while at the wafer level and then slicing it into chips to make the completed product, which differs from the conventional method of slicing the processed wafer first into individual chips and then packaging them. WLCSP is a true chip-scale packaging technology.

Demand for WLCSP is increasing rapidly in the mobile market, due to the realization of a true chip-scale package with excellent electrical properties and price competitiveness. The WLCSP continues to expand its scope of application.

LB Semicon currently provides various layers of WLCSP solutions ranging from two layers to six layers tailored to meet the needs of our customers

Features
• 8inch and 12inch available
• Large die WLCSP qualified up to 6x6m, Small die WLCSP down to 0.5 x 0.5mm available with high and stable TnR(Tape and Reel) yield
• Thick RDL and UBM are available up to 20um for power management IC required to apply high current with low Rdson.
• Capable of Ball drop > 0.3mm pitch as well as Electroplated bumping for thin package profile
• PBO and PI for Re-passivation
• Low temperature curable PI ready for thermal sensitive device like Nand fresh memory
• Laser grooving available for < 65nm technical node
• Die silicon thickness ranges from 720um to 150um

Application
• PMIC, DMB RF & BB SoC, Transceiver, AOC, Sensors..
WLCSP stack-up Option

1P1M

- The most simplified WLCPS structure.
  - Solder balls are directly placed on I/O pad without RDL
  - I/O pad must be located where the ball is supposed to be placed on

2P1M

- Cost effective and fast cycle time compared to 2P2M
  - I/O pads are relocated by Cu RDL to fit JEDEC standard pitch and then solder ball are attached on RDL

2P2M

- Standard WLCSP structure most widely used in industry
  - I/O pads are relocated by Cu RDL to fit JEDEC standard pitch and Solder ball are mounted on Cu UBM
  - Provide the best reliability performance
  - Thick RDL and UBM available up to 20um (30um RDL will be released in the end of 2017)

2P2M_RDL option

10um RDL (In mass production)

20um RDL (Qualified)

30um RDL (under qualification)
High I/O density and
- I/O pads are relocated by dual RDL
- Enable High I/O density IC which is designed for purpose of wire package easy switching to WLCSP

Process capability
- Bumping process
  - Ball pitch: 0.3, 0.35, 4.0, 5.0mm
  - Ball Height
    - Ball drop: > 0.15mm
    - Electroplated: < 0.11mm
  - Re-PSV thickness: 5 to 30um
  - Re-PSV opening diameter
    - PBO: > 15um
    - PI: > 30um
  - RDL thickness: 3mm to 20um
  - RDL line/width (min): 15mm/15um
- Backend process
  - Back-grinding for wafer thinning: > 0.15mm
  - Backside coating: available
  - Scribe lane for dicing: 60um (laser grooving available)
  - Die size (min): 0.5mm x 0.5mm
Materials Information

- Polymeric Re-passivation: PI and PBO
- RDL (Redistribution layer): Electroplated Copper
- UBM: Electroplated Copper, Nickel
- Ball
  - Ball drop: SAC105, 305, 405 and LF35
  - Electroplated: Lead free solder (SnAg1.8%)
- Backside coating film: LC2850

Reliability

- Moisture Sensitivity: JEDEC LEVEL 1 @ 260°C
- Temperature Cycling: -65°C/150°C, 500 cycles
- High Temperature Storage: 150°C, 1000 hours
- Highly Accelerated Temperature and Humidity Stress: 130°C/85% RH, 96 hours

Questions? Contact us: marketing@lbsemicon.com