Overview
As semiconductor devices are rapidly becoming more integrated and faster, chip’s I/O density is increasing at a rapid pace while the bump pitch is continuously decreasing. Cu pillar is a bumping technology, developed to meet such needs for fine pitches, and it can accomplish much finer pitch of 40μm or smaller, compared to the 150μm level that existing Solder bumping method could reach. Cu pillar is currently being applied to various packages and its application will be expanded even more because of its excellent thermal dissipation performance and electromigration properties, compared to Solder bumping.

Benefit
- Fine pitches possible down to 40μm
- High electrical and thermal conductivity
- Better thermal cycling and electromigration reliability performance than solder
- Smaller bump pitches than solder bumps help resolve I/O limitation issues of newer CMOS nodes
- Larger spacing between adjacent bumps for signal routing and easier underfill flow
- High bump aspect ratio (easier underfill flow)

Cu pillar bump with lead free solder cap

Application
- fcBGA and fcQFN package for RFIC, BB & AP processor, Power Amplifiers, NAND Flash, WiFi module..
**Cu pillar Option**

**CuP_1M**
- Cu pillar is directly placed on I/O Pad
- Both SMD and NSMD are available

**NSMD**

**SMD**

**Cup_1P1M**
- Polymeric Re-passivation is coated on a wafer prior to Cu pillar bumping as a stress buffer layer and then Cu pillar is formed on I/O Pad.
- Provide better reliability performance

**Cup_2P2M**
- RDL option is available if necessary to rout I/O pad.
- Thick RDL is feasible up to 20um.
Process capability

- 8inch and 12inch wafer available.
- Cu pillar option
  - Direct CuP (1M)
  - CuP on polymeric re-passivation (1P1M)
  - CuP with electroplated Cu RDL (2P2M)
- Cu pillar pitch and Total height
  - Pitch(min)
    - 50um pitch for 8inch
    - 40um pitch for 12inch
  - Total height : 30 ~ 90um (depending on Cu pillar diameter and Pitch)
- Cu Pillar material stack-up option
  - Cu post / Solder cap
  - Cu post / Ni barrier metal / Solder Cap (Provide better kirkendall void performance)

Materials Information

- Polymeric Re-passivation
  - High temperature curable : PI and PBO
  - Low Temperature Curable : Epoxy and Novolak based dielectrics
- UBM : TiW/Cu or Ti Cu
- Solder Cap : Electroplated lead free solder (SnAg1.8%)
- RDL(Redistribution) : Electroplated Cu
Design rule

Cu Pillar Bump

[NSD structure]

[NSD structure]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Design Rule (unit: um)</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>40um pitch</td>
</tr>
<tr>
<td>A1</td>
<td>Cu pillar diameter (maximum)</td>
<td>25</td>
</tr>
<tr>
<td>A2</td>
<td>Cu post height (maximum)</td>
<td>40</td>
</tr>
<tr>
<td>A3</td>
<td>Solder cap height (maximum)</td>
<td>13</td>
</tr>
<tr>
<td>A4</td>
<td>Total Cu pillar height (maximum)</td>
<td>53</td>
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<tr>
<td>A5</td>
<td>Distance between bumps (minimum)</td>
<td>15</td>
</tr>
<tr>
<td>A6</td>
<td>Distance from passivation open edge to Bump edge (minimum)</td>
<td>3</td>
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Questions? Contact us: marketing@lbsemicon.com